

EXHIBIT 21

FILED UNDER SEAL

UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

NETLIST, INC.,)
)
Plaintiff,)
)
vs.)Case No.
)2:22-cv-203-JRG
MICRON TECHNOLOGY, INC.,)
MICRON SEMICONDUCTOR)
PRODUCTS, INC., and MICRON)
TECHNOLOGY TEXAS, LLC,)
)
Defendants.)
)

REMOTE VIDEOTAPED DEPOSITION
OF

JOHN BENTLEY HALBERT, III
Saturday, September 30, 2023
Castiglione Falletto, Italy

Reported by: B. Suzanne Hull, CSR No. 13495

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1	APPEARANCES	1	EXHIBITS (Continued)
2		2	EXHIBIT DESCRIPTION PAGE
3		3	Exhibit 31 MIPI M-PHY future mobile PHY 46
4	For Plaintiff: Irell & Manella, LLP	4	proposal, September 2009,
5	By MS. HONG (ANNITA) ZHONG	5	Bates Stamp Numbers
6	Attorney at Law	6	SAM-NET00061251 through
7	1800 Avenue of the Stars	7	SAM-NET00061288, JC42.6 Item
8	Suite 900	8	Number 1776.10, thirty-eight
9	Los Angeles, California 90067	9	pages
10	(310) 203-7183	10	Exhibit 32 Wide-IO TG report, 46
11	hzhong@irell.com	11	December 2009, FM-Mobile Wide
12	For Defendants: Winston & Strawn LLP	12	IO TG, Bates Stamp Numbers
13	By MR. VIVEK V. KRISHNAN	13	SAM-NET00065075,
14	Attorney at Law	14	SAM-NET00065087, Item Number
15	35 West Wacker Drive	15	1777.00, thirteen pages
16	Chicago, Illinois 60601	16	Exhibit 33 Advanced memory package 46
17	(312) 558-9508	17	proposal, Item Number 1782.01,
18	vkrishnan@winston.com	18	1st showing, March 2010,
19		19	Bates Stamp Numbers
20		20	SAM-NET00067316 through
21		21	SAM-NET00067322, seven pages
22		22	///
23		23	///
24		24	///
25		25	///
Page 2		Page 4	
1	I N D E X	1	EXHIBITS (Continued)
2		2	EXHIBIT DESCRIPTION PAGE
3	EXAMINATION BY PAGE	3	Exhibit 34 FMD - Wide I/O TG read clock 46
4		4	proposal, March 2010,
5	MS. ZHONG 10	5	Sponsored by Apple/Hynix,
6		6	Bates Stamp Numbers
7		7	SAM-NET00068554 through
8		8	SAM-NET00068559, six pages
9	E X H I B I T S	9	Exhibit 35 Wide I/O ball map baseline 47
10		10	proposal, first showing,
11	EXHIBIT DESCRIPTION PAGE	11	Sponsors: Elpida, Intel,
12	Exhibit 2 Micron prior art - public 14	12	Nokia, Samsung, June 7, 2010,
13	availability dates, two pages	13	Item Number 1777.29,
14	Exhibit 1 Slide deck, Introduction to 16	14	Bates Stamp Numbers
15	JEDEC, March 2023, Bates Stamp	15	SAM-NET00072684 through
16	Numbers MICNL203_00082326	16	SAM-NET00072687, four pages
17	through MICNL203_00082386,	17	Exhibit 36 Future Mobile Memory (FMM), 47
18	sixty-one slides	18	Wide I/O refresh scheme,
19	Exhibit 3 Expert report of 27	19	second showing, Item Number
20	John B. Halbert, dated	20	1777.18, September 10, 2010,
21	December 22, 2022,	21	Bates Stamp Numbers
22	twenty-eight pages	22	SAM-NET00076461 through
23	Exhibit 4 Deposition of John Bentley 30	23	SAM-NET00076463, three pages
24	Halbert, III, dated July 22,	24	///
25	2022, seventy pages	25	///
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1	EXHIBITS (Continued)		1	Castiglione Falletto, Italy	
2	EXHIBIT DESCRIPTION PAGE		2	Saturday, September 30, 2023; 4:06 p.m.	
3	Exhibit 37 Future high bandwidth memory 47		3	Villa Roma 29	
4	TG, Item Number 1797.00,		4		
5	TG42_1: TG report, June 2011,		5	THE VIDEOGRAPHER: Good afternoon.	
6	Vancouver, Bates Stamp Numbers		6	We are on the record. 16:06:04	
7	SAM-NET00090212 through		7	The time is 4:06 p.m. That is 16:06:05	
8	SAM-NET00090229, eighteen		8	Central European Time. 16:06:12	
9	pages		9	The date today, September 30th, 2023. 16:06:14	
10	Exhibit 38 TSV tile memory clocking and 47		10	Please note that this deposition is being 16:06:18	
11	command, second showing,		11	conducted virtually.	
12	Item Number 178705,		12	Quality of recording depends on the quality	
13	April 21/22, 2011, TG,		13	of camera and Internet connection of participants.	
14	Advantest, Avago, LSI, Nanya,		14	What is seen from the witness and heard on	
15	SAM-NET00090380 through		15	screen is what will be recorded.	
16	SAM-NET00093084, five pages		16	Audio and video recording will continue to	
17	Exhibit 39 Future high bandwidth memory 47		17	take place unless all parties agree to go off the	
18	TG, Item Number 1797.00,		18	record.	
19	TG42_1: TG report,		19	This is media unit one of the video-recorded 16:06:36	
20	September 2011, Chicago,		20	deposition of John Halbert taken by counsel for 16:06:40	
21	Bates Stamp Numbers		21	plaintiff in the matter of Netlist, Inc., versus 16:06:44	
22	SAM-NET00094393 through		22	Micron Technology, Inc., et al., filed in 16:06:49	
23	SAM-NET00094412, twenty pages		23	United States District Court, for the Eastern 16:06:51	
24	///		24	District of Texas, Marshall Division, Case Number 16:06:54	
25	///		25	2:22-cv-203-JRG. 16:06:56	
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1	EXHIBITS (Continued)		1	The deposition is being conducted remotely 16:06:58	
2	EXHIBIT DESCRIPTION PAGE		2	using virtual technology. 16:07:04	
3	Exhibit 40 A stackable, configurable 47		3	My name is David West. I am the 16:07:05	
4	memory sheet for ASICs:		4	videographer. The court reporter is Suzanne Hull. 16:07:07	
5	A first showing, Item Number		5	We represent Veritext Legal Solutions. 16:07:09	
6	1787.01, Bates Stamp Numbers		6	I am not related to any party in this 16:07:11	
7	SAM-NET00321291 through		7	action, nor am I financially interested in the 16:07:14	
8	SAM-NET00321301, eleven pages		8	outcome. 16:07:17	
9	Exhibit 11 DDR4 LRDIMM proposal, Item 70		9	If there are any objections to proceeding, 16:07:17	
10	Number 158.01, Second showing,		10	please state them at the time of your appearance. 16:07:20	
11	Intel, Bates Stamp Numbers		11	Counsel will now state their appearances and 16:07:22	
12	SAM-NET00321470 through		12	affiliations for the record, beginning with the 16:07:25	
13	SAM-NET00321472, three pages		13	noticing attorney. 16:07:28	
14	Exhibit 5 United States Patent, Halbert, 71		14	MS. ZHONG: Annita Zhong, from 16:07:28	
15	et al., Patent Number US		15	Irell & Manella, representing the plaintiff, Netlist, 16:07:30	
16	7,024,518 B2, date of patent:		16	Inc. 16:07:34	
17	April 4, 2006, twenty pages		17	MR. KRISHNAN: Vivek Krishnan, of 16:07:35	
18	Exhibit 27 FBDIMM specification: DDR2 89		18	Winston & Strawn, on behalf of Micron and the 16:07:37	
19	SDRAM fully buffered DIMM		19	witness. 16:07:42	
20	(FBDIMM) design specification,		20	THE VIDEOGRAPHER: Thank you. 16:07:43	
21	one hundred twenty-nine pages		21	The court reporter may now swear the witness 16:07:44	
22			22	in, and we will continue. 16:07:47	
23			23	THE REPORTER: Raise your right hand, 16:07:49	
24			24	please, sir. 16:07:51	
25			25	Do you solemnly swear or affirm that the 16:07:52	
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1	MR. KRISHNAN: Objection. Form.	19:12:31	1	BY MS. ZHONG:	19:14:38
2	THE WITNESS: Yeah.	19:12:34	2	Q. Okay.	19:14:38
3	You could say that wire bond was the most	19:12:35	3	A. -- in that time frame.	19:14:38
4	common.	19:12:38	4	Q. But you don't know for sure?	19:14:40
5	BY MS. ZHONG:	19:12:38	5	A. No.	19:14:45
6	Q. Okay. At least in 2009 to 2010 time period	19:12:38	6	Because it has been too long.	19:14:45
7	the wire bond connection is -- was the most common	19:12:44	7	Q. Okay. Can you use a DRAM circuit in DDRs,	19:14:48
8	for the dual die package and the quad die package; is	19:12:48	8	LRDDRs for HBM?	19:15:29
9	that correct?	19:12:51	9	MR. KRISHNAN: Objection. Form.	19:15:33
10	MR. KRISHNAN: Objection. Form.	19:12:52	10	THE WITNESS: What -- what are you asking?	19:15:36
11	THE WITNESS: Yes.	19:12:53	11	BY MS. ZHONG:	19:15:38
12	Wire bond was probably the most common.	19:12:55	12	Q. Okay.	19:15:38
13	BY MS. ZHONG:	19:12:55	13	A. You are mixing a bunch of terms together.	19:15:39
14	Q. Okay. So for those wire-bonded packages,	19:12:58	14	Q. Okay. Can you use a DRAM circuit in DDR2?	19:15:41
15	would the electrical and the mechanical con- -- would	19:13:03	15	A. What do you define as DRAM circuits?	19:15:51
16	the electrical connection for an upper die go through	19:13:06	16	Q. What is your understanding of the term DRAM	19:15:55
17	the lower die?	19:13:13	17	circuit?	19:15:57
18	MR. KRISHNAN: Objection. Form.	19:13:15	18	A. I think it -- you are the one asking the	19:15:58
19	THE WITNESS: The fact that it is wire bond	19:13:17	19	question. You are -- you need to clarify what your	19:16:01
20	would say that the wires connecting the upper die	19:13:21	20	question is.	19:16:04
21	would go down to the package.	19:13:25	21	Q. Okay. Is there -- is the word DRAM circuit	19:16:05
22	BY MS. ZHONG:	19:13:27	22	a term of art?	19:16:08
23	Q. Okay. Was -- without going through the	19:13:27	23	A. A term of the art? No.	19:16:10
24	lower die?	19:13:29	24	Q. So what is your understanding of DRAM	19:16:13
25	MR. KRISHNAN: Objection. Form.	19:13:30	25	circuit?	19:16:18
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1	THE WITNESS: Correct.	19:13:34	1	A. So a DRAM circuit --	19:16:19
2	BY MS. ZHONG:	19:13:36	2	MR. KRISHNAN: Objection. Form.	19:16:22
3	Q. Okay. And you mentioned earlier that there	19:13:36	3	THE WITNESS: From a design point of view,	19:16:23
4	were connections -- there were manufacturers that	19:13:38	4	a DRAM circuit would be anything outside of the cell	19:16:26
5	connect the die along the outside edge of the die.	19:13:46	5	array that only contains memory cells; so a DRAM	19:16:29
6	Were those down in the 2009 to 2010 period?	19:13:51	6	circuit would include the sense sound, the column	19:16:34
7	MR. KRISHNAN: Objection. Form.	19:13:58	7	decoder, the row decoder. And maybe even the	19:16:38
8	THE WITNESS: That is a good question.	19:13:59	8	secondary sense amps along the I/O are all DRAM	19:16:42
9	There was --	19:14:00	9	circuits that are only used in DRAMs.	19:16:47
10	BY MS. ZHONG:	19:14:00	10	BY MS. ZHONG:	19:17:06
11	Q. I don't -- not when was it done? When did	19:14:00	11	Q. Are the same DRAM circuits used for	19:17:07
12	they start to do it? Maybe that is a better	19:14:05	12	different types of DRAM devices?	19:17:10
13	question.	19:14:07	13	A. So all -- well, kind of put that in quotes.	19:17:15
14	A. I don't remember. Everything kind of blurs	19:14:08	14	Let's say 99 percent of anything that has DRAM cells	19:17:21
15	together back then. There were a lot of different	19:14:10	15	will have DRAM circuits included. Like I mentioned,	19:17:28
16	technologies being proposed and produced to create	19:14:13	16	sense amps, column decoders, row decoders, secondary	19:17:34
17	a better stack.	19:14:18	17	sense amps.	19:17:42
18	Q. Okay.	19:14:19	18	Q. Okay. What about circuits for IEEE testing?	19:17:43
19	A. So whether it was 2009-'10, I don't	19:14:19	19	A. Uh-huh.	19:17:56
20	remember. Or earlier.	19:14:24	20	Q. Do they have -- are those DRAM circuits?	19:17:58
21	Q. Do you know whether it is -- it was done by	19:14:24	21	MR. KRISHNAN: Objection. Form.	19:18:04
22	2011-2012?	19:14:27	22	THE WITNESS: That is kind of a goofy	19:18:06
23	MR. KRISHNAN: Objection. Form.	19:14:34	23	question.	19:18:12
24	THE WITNESS: My guess it probably was --	19:14:35	24	BY MS. ZHONG:	19:18:12
25	///		25	Q. Okay.	19:18:12
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<p>1 A. I mean, it is like trying to mix apples and 19:18:13 2 oranges. 19:18:17 3 Q. Okay. 19:18:18 4 A. So you are saying -- are you asking if JTAG 19:18:18 5 is used on DRAMs? 19:18:25 6 Q. JTAG? J-T-A-G? 19:18:28 7 A. Yeah. 19:18:39 8 Q. Yes. 19:18:39 9 So my understanding is that HBM has pretty 19:18:39 10 advanced testing capabilities in them. 19:18:45 11 Is that your understanding as well? 19:18:48 12 A. Yes. 19:18:51 13 MR. KRISHNAN: Objection to form. 19:18:51 14 BY MS. ZHONG: 19:18:53 15 Q. Okay. So -- so there has got to be testing 19:18:53 16 circuits in the HBM packages; correct? 19:18:58 17 MR. KRISHNAN: Objection to form. 19:19:03 18 THE WITNESS: There are testing circuits -- 19:19:04 19 yeah. 19:19:04 20 There are testing circuits in HBM packages. 19:19:05 21 They are also testing circuits on each die in the 19:19:10 22 stack. 19:19:14 23 BY MS. ZHONG: 19:19:15 24 Q. Okay. So are those testing circuits what 19:19:15 25 you call -- what -- what you would refer to as DRAM 19:19:18 Page 122</p>	<p>1 stack or they are a mono die. 19:21:13 2 Q. Okay. But are there testing circuits unique 19:21:17 3 to the HBM products? 19:21:24 4 MR. KRISHNAN: Objection. Form. 19:21:25 5 THE WITNESS: Yes. 19:21:27 6 So there is an IEEE 1500 bus on the base 19:21:38 7 die. There is also -- there is probably other -- 19:21:43 8 there is testing circuits for checking the connection 19:21:49 9 between the base die and the vols in the package; so 19:21:53 10 those -- those would be unique to HBM. But I believe 19:21:59 11 there are other die that have -- or other standards 19:22:07 12 that have copied that for DRAM that have many 19:22:10 13 outputs. 19:22:15 14 BY MS. ZHONG: 19:22:15 15 Q. Okay. So let's stay on that. 19:22:16 16 Is the IEEE testing circuits on both the 19:22:20 17 logic die, as well as the DRAM device die? 19:22:27 18 A. No. 19:22:31 19 Q. So there are no corresponding circuits on 19:22:31 20 the memory die? 19:22:41 21 A. For an IEEE 1500 bus, no. Because that is 19:22:42 22 used to -- as a method to address the stack once it 19:22:49 23 is all put together. 19:22:54 24 Q. Are you saying the circuit only exists on 19:22:55 25 the logic die but not on the DRAM die? 19:23:05 Page 124</p>
<p>1 circuits? 19:19:22 2 MR. KRISHNAN: Objection. Form. 19:19:24 3 THE WITNESS: So, again, you are, kind of -- 19:19:25 4 you are trying to twist terms around, which makes it 19:19:38 5 very difficult to answer the question. If your 19:19:42 6 question is are there common testing circuits between 19:19:45 7 the die and the HBM stack and in the base die and in 19:19:51 8 monolithic -- i.e., DDR3 or DDR4 -- the answer is 19:19:58 9 yes. 19:20:06 10 BY MS. ZHONG: 19:20:07 11 Q. Are there unique testing circuits for the 19:20:12 12 HBM products? 19:20:16 13 MR. KRISHNAN: Objection. Form. 19:20:20 14 THE WITNESS: Hmmm. It depends on which 19:20:21 15 testing circuits we're talking about. Some are 19:20:25 16 common between monolithic DRAMs, DDR3 and HBM, 19:20:31 17 especially at the die test level. 19:20:43 18 BY MS. ZHONG: 19:20:45 19 Q. Uh-huh. 19:20:45 20 A. And so the die and the stack -- in the HBM 19:20:46 21 stack have to have I/O circuits that allow the test 19:20:49 22 machine to test all of the DRAM cells. And because 19:20:54 23 there are so many cells, there are test circuits that 19:20:58 24 test many cells in parallel. This is a common method 19:21:04 25 used in testing DRAMs, whether they are in the HBM 19:21:09 Page 123</p>	<p>1 MR. KRISHNAN: Objection. Form. 19:23:09 2 THE WITNESS: So IEEE 1500 is a testing 19:23:10 3 standard that has lots of functionality to it. JTAG, 19:23:15 4 as I mentioned -- J-T-A-G -- is a simpler method of 19:23:27 5 testing, less robust. It may or may not be included 19:23:30 6 by the memory suppliers on the mono die as a method 19:23:38 7 to reduce the number of connections that they have to 19:23:44 8 make to the die when it is in wafer form; so it could 19:23:47 9 very well be a version of a serial access to the die 19:23:52 10 in the stack. But I can't answer that because that 19:23:59 11 would be a supplier -- and we call it secret sauce. 19:24:02 12 BY MS. ZHONG: 19:24:09 13 Q. Okay. So if there is an IEEE 1500 testing 19:24:10 14 circuit on the DRAM die, that would be unique to the 19:24:16 15 HBM DRAM and is absent from monolithic PDRs; is that 19:24:23 16 right? 19:24:31 17 MR. KRISHNAN: Objection. Form. 19:24:32 18 THE WITNESS: There is no reason to 19:24:36 19 include -- as I said, IEEE 1500, it is a very robust 19:24:37 20 serial bus access to the -- 19:24:47 21 BY MS. ZHONG: 19:24:49 22 Q. Uh-huh. 19:24:49 23 A. -- die. It is used in other chips, probably 19:24:50 24 CPUs. There is no -- if you have a die that only 19:24:54 25 has, what, sixteen I/Os -- 19:24:58 Page 125</p>